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T. BELL
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

CETIN KAYA

Serial No. 09/620,649 (TI-23686.1)

Filed July 20, 2000

For: INTEGRATED CIRCUIT HAVING INDEPENDENTLY FORMED ARRAY AND PERIPHERAL ISOLATION DIELECTRICS

Art Unit 2822

Examiner D. Goodwin

Commissioner for Patents
Washington, D. C. 20231

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 12 to 19, all of the rejected claims. Claim 20 has been indicated to be allowable and claims 1 to 11 were the subject matter of the parent application, now issued.

Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

A response and Declaration were filed after final rejection and were apparently entered for purposes of appeal.

SUMMARY OF INVENTION

The invention relates to an integrated circuit (10) having a first dielectric layer (20) disposed outwardly from a substrate (12). A plurality of gate stacks (22) are provided, each gate stack having a floating gate body (24) disposed outwardly from the first dielectric layer, a second dielectric region (28) disposed outwardly from the floating gate body and a first polysilicon layer (26) disposed outwardly from the second dielectric region. A plurality of dielectric isolation regions (30) are disposed between the gate stacks, the dielectric isolation regions formed after the formation of the gate stacks. Each dielectric isolation region may include an isolation oxide layer (32) and an isolation dielectric layer (34), the dielectric isolation region formed by growing the isolation oxide layer outwardly from the gate stacks, depositing the isolation dielectric layer outwardly from and between the gate stacks; and removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer. The dielectric isolation regions can be formed by growing approximately 200Å of oxide outwardly from the gate stacks, depositing approximately 0.5 micrometers of oxide outwardly from and between the gate stacks and removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer. Each floating gate body can have a rough outer surface.

ISSUE

The sole true issue on appeal is whether appellant has properly antedated the reference to Van Buskirk (U.S. 6,001,689) sufficient to remove this reference as an applicable reference under 35 U.S.C. 102 or 103 against claims 12 to 19.

GROUPING OF CLAIMS

The claims on appeal stand or fall together.

ARGUMENT

Claims 12, 13, 15 and 16 were rejected under 35 U.S.C. 102(e) as being anticipated by Van Buskirk (U.S. 6,001,689), claims 14 and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk in view of Chan (U.S. 6,051,467) and claims 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk in view of Woo (U.S. 5,926,711). Since the issue in each case is the same, the argument as to each of the three rejections is combined. The rejections are without merit.

The provisional application upon which the subject application is based and which contains the same disclosure as the subject application was not filed within a year prior to the filing of the parent application, the hiatus being seven days. The facts as presented demonstrate, even without requirement of further declaration since all facts are on the record, that a conception and reduction to practice with diligence from conception to reduction to practice is present in this case. It is clear and cannot be disputed from the record that the provisional application was filed September 30, 1997, this date being prior to the filing date of Van Buskirk. It is also clear and cannot be disputed from the record that the parent of the subject application was filed October 7, 1998, seven days subsequent to the statutory requirement for claiming

priority under 35 U.S.C. 119. It further cannot be disputed that the provisional application is substantially identical to if not identical to the subject application. It follows that the filing of the provisional application initially provided a constructive reduction to practice for a parent application to be subsequently filed or at least provided diligence after a conception with the filing of the parent of the subject application being either a second constructive reduction to practice or a first constructive reduction to practice after the conception with diligence (diligence being the filing and continued pendency of the provisional application). It follows that the only break in the continuum was the seven day period noted above between the end of one year subsequent to filing of the provisional application and the filing of the parent of this application. This short break in the continuum does not amount to a failure of the diligence already completed as evidenced by the decision in Keizer v. Bradley, 270 F.2d 396, 397, 123 USPQ 215, 216 (CCPA 1959) wherein it is stated that "'attorney -diligence' and 'engineering-diligence'...does not require than 'an inventor or his attorney...drop all other work and concentrate on the particular invention involved...' (Emery v. Ronden, 188 USP! 264, 268 (Bd. Inter. 1974).'" as stated at MPEP 2138.06. It follows that Van Buskirk is still not available as a reference under 35 U.S.C. 102 or 103 in this case.

Though all of the above facts are of record in the records of the Patent and Trademark Office ab initio, the undersigned, out of an abundance of caution, also presented the above facts in Declaration form.

The Advisory Action in the subject application states that a Declaration under 35 U.S.C. 1.131 is required and that "the 7 day period for which diligence is required must be accounted for by either affirmative acts or acceptable excuses". These requirements are nowhere supported by law and no support therefor has been provided. In fact, these requirements are clearly contrary to

the express provisions of the M.P.E.P. as set forth above. A declaration under 35 U.S.C. 1.131 is required to show facts proving conception with diligence or reduction to practice prior to the effective date of a reference. No such facts need be established in this case since the facts of record in the Patent and Trademark Office clearly establish these facts. Furthermore, out of an abundance of caution, the undersigned provided a Declaration (the response after final rejection) setting forth the pertinent facts, though no such declaration is believed to have been necessary. With reference to the requirement to show diligence for the 7 day period (the hiatus discussed above), again, no such showing is required since the record shows a constructive reduction to practice prior to the effective filing date of Van Buskirk and it is further clear that for a seven day hiatus there is no lack of diligence as noted in the above case law. Clearly, the failure to file the parent of the subject application within one year of the filing of the provisional application was due to inadvertent, the cause of which cannot be determined.

It is clear from the records available in the Patent and Trademark Office ab initio that it has been established that the subject matter of the subject application was conceived and constructively reduced to practice prior to the effective filing date of Van Buskirk. Accordingly, the Van Buskirk patent is not an applicable reference in this case and the rejection of claims 12 to 19 based totally or in part on Van Buskirk is without merit.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

12. An integrated circuit, comprising:

a first dielectric layer disposed outwardly from a substrate;

a plurality of gate stacks, each gate stack comprising:

a floating gate body disposed outwardly from the first dielectric layer;

a second dielectric region disposed outwardly from the floating gate body; and

a first polysilicon layer disposed outwardly from the second dielectric region; and

a plurality of dielectric isolation regions disposed between the gate stacks, the dielectric isolation regions disposed between the gate stacks, the dielectric isolation regions formed after the formation of the gate stacks.

13. The integrated circuit of Claim 12, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

the dielectric isolation region formed by growing the isolation oxide layer outwardly from the gate stacks;

depositing the isolation dielectric layer outwardly from and between the gate stacks; and removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

14. The integrated circuit of Claim 12, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

the dielectric isolation region formed by:

growing approximately 200Å of oxide outwardly from the gate stacks;

depositing approximately 0.5 micrometers of oxide outwardly from and between the gate stacks; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

15. The integrated circuit of Claim 12, wherein the substrate comprises at least one trench disposed between two gate stacks; and

at least one moat disposed adjacent to the at least one trench and inwardly from the at least one gate stack.

16. The integrated circuit of Claim 15, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

the dielectric isolation region formed by:

growing a layer of oxide outwardly from the gate stacks;

depositing a dielectric outwardly from and between the gate stacks and outwardly from the trenches in the substrate; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

17. The integrated circuit of Claim 12, wherein each second dielectric region comprises a layer of oxide having a thickness of approximately 70Å.

18. The integrated circuit Claim 12, wherein each gate stack further comprises a hemispherical grain poly layer disposed outwardly from the floating gate body.

19. The integrated circuit of Claim 12, wherein each floating gate body comprises a rough outer surface.